

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Yi Ding
Assignee: Mosel Vitelic, Inc.
Title: Arrays of Nonvolatile Memory Cells Wherein Each Cell Has Two Conductive Floating Gates
Application No.: Unassigned Filing Date: Filed Herewith
Examiner: Unassigned Group Art Unit: Unassigned
Docket No.: M-15223 US

San Jose, California
July 30, 2003

Mail Stop Patent Application
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR § 1.97(b)

Dear Sir:

Pursuant to 37 CFR § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be material to patentability as defined in § 1.56(b).

No fee is believed to be required. If a fee is required for this Information Disclosure Statement, please charge the fee to Deposit Account No. 50-2257. This paper is being submitted in duplicate.

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Respectfully submitted,

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U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.	Serial No.		
				M-15223 US	Unassigned		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)				Applicant(s)			
				Yi Ding			
				Filing Date	Group		
				Filed Herewith		Unassigned	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,402,371	28 Mar. 1995	Ono			
	AB	5,856,943	5 Jan. 1999	Jenq			
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	AD	6,130,129	10 Oct. 2000	Chen			
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	AL	Shirota, Riichiro "A Review of 256Mbit NAND Flash Memories and NAND Flash Future Trend," February 2000, Nonvolatile Memory Workshop in Monterey, California, pages 22-31.					
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	AO	Mizutani, Yoshihisa; and Makita, Koji "A New EPROM Cell With A Sidewall Floating Gate Fro High-Density and High Performance Device," 1985 IEEE, 635-638.					
	AP	Ma, Y.; Pang, C.S.; Pathak, J.; Tsao, S.C.; Chang, C.F.; Yamauchi, Y.; Yoshimi, M. "A Novel High Density Contactless Flash Memory Array Using Split-Gate Source-Side-Injection Cell for 5V-Only Applications," 1994 Symposium on VLSI Technology Digest of Technical Papers, pages 49-50.					
	AQ	Mih, Rebecca et al. "0.18um Modular Triple Self-Aligned Embedded Split-Gate Flash Memory," 2000 Symposium on VLSI Technology Digest of Technical Papers, pages 120-121.					
	AR	Ma, Yale et al., "A Dual-Bit Split-Gate EEPROM (DSG) Cell in Contactless Array for Single Vcc High Density Flash Memories," 1994 IEEE, 3.5.1-3.5.4.					
Examiner		Date Considered					
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

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				Filed Herewith		Unassigned	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AS	6,437,360	20 Aug. 2002	Cho et al.			
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	BE	Kim, K.S. et al. "A Novel Dual String NOR (DuSnor) Memory Cell Technology Scalabe to the 256 Mbit and 1 Gbit Flash Memories," 1995 IEEE 11.1.1-11.1.4					
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	BG	Van Duuren, Michiel et al., "Compact poly-CMP Embedded Flash Memory Cells For One or Two Bit Storage," Philips Research Leuven, Kapeldreef 75, B3001 Leuven, Belgium, pages 73-74.					
	BH						
	BI						
	BJ						
Examiner		Date Considered					
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